A LOW CURRENT, HIGH GAIN MONOLITHIC AMPLIFIER COVERING 5-20 GHz BANDWIDTH

HORNG-JYE SUN, AND PHILIP A. TERZIAN

NARDA WESTERN OPERATIONS
214 Devcon Drive
San Jose, CA 95112

ABSTRACT

A monolithic amplifier has been developed using a three-stage structure with feedback input/output stages and a reactively matched middle stage. The amplifier has exhibited greater than 12dB gain across 5-20 GHz bandwidth at a bias current of 40mA. The current to gain efficiency of 3.3mA/dB is the highest ever reported for a monolithic amplifier covering this bandwidth. The VSWR is less than 2.0:1 at input and less than 2.5:1 at output. The middle stage also provides a separate gain control with greater than 10dB dynamic range.

INTRODUCTION

In recent years, broadband monolithic amplifier designs have made significant progress. The applications for these amplifiers generally require ICs with small size, broadband, high gain, and low current consumption. To achieve the broadband requirement, most designs have used the distributed-amplification approach (1). Yet the DC current to gain efficiency of this approach is generally poor, being about 10mA/dB (2, 3, 4). Furthermore, most of the distributed designs require complex processing, such as 0.25u gate length, dual-gate devices or via-hole grounding to achieve that gain efficiency. A feedback design will have higher DC current to gain efficiency. A recent design (5) using two feedback stages has shown 5mA/dB current to gain efficiency over 6-18 GHz, though the input/output matches preclude direct cascading of chips. In this paper, the development of a monolithic amplifier is presented that is capable of low current, high gain, fair VSWR, high reverse isolation, and a separate AGC port, over 5-20 GHz bandwith.

AMPLIFIER DESIGN

The design uses a three-stage circuit topology with feedback input and output stages and a reactively matched middle stage (Figure 1). The input and output stages provide the I/O matches. The reactive middle stage yields higher amplifier gain and reverse isolation. Thus the input and output stages focus on amplifier VSWR reduction and the middle stage is used to adjust gain ripple. In addition, a feedback design normally does not have enough gain at the high frequency end, which may affect the IC yield. The inclusion of a reactive stage can offset this drawback. This is demonstrated by the performance of the present design which covers 5-20 GHz bandwidth. The middle stage also adds an extra AGC port, separate from the input and output stages, reducing the effect of the AGC on the amplifier input and output stages.

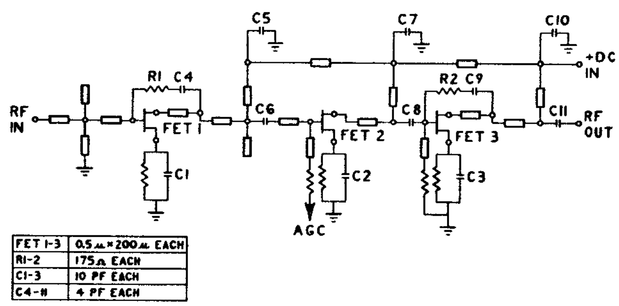


FIGURE 1 SCHEMATIC DIAGRAM OF THE 5-20 GHZ HIGH GAIN MONOLITHIC AMPLIFIER

The monolithic IC uses three 0.5u x 200u MSEFETs (one/stage). The device size was chosen based on gain, bandwidth, and current consumption considerations. Each stage is self-biased to facilitate the use of a single power supply and all DC bias circuits are included on chip. MIM capacitors are used for DC blocking and RF bypassing, eleven capacitors with total capacitance of 62 pF are included on the IC. Spiral inductors (a total of six) are employed in non critical locations to reduce the chip size. These inductors range from 1.0nh to 3.5nh (measured at 1 GHz). A lumped equivalent circuit, including parasitic R, L, and C and verified to be valid up to 23 GHz, was used to model these inductors. Extensive sensitivity analyses were performed during circuit design to identify critical elements. The results were then used in the design and also used for process control.

IC FABRICATION

The IC fabrication comprises mesa isolation, recessed Ti/Pt/Au gates, CVD silicon nitride (for FET passivation and MIM capacitor formation), mesa and thin-film metal resistors, and air-bridge interconnects. The mesa resistors (with sheet resistance of about 650 ohms per square) are used for DC-bias applications, while the metal resistors (with sheet resistance about 7.5 ohms per square) are used for tight tolerance applications such as the feedback resistors. The latter have better uniformity control across the wafer and over different lots. The fabricated feedback resistors, with resistance of about 175 ohms, have exhibited a standard deviation of less than 5%.

The wafer was backlapped to a thickness of 5 mils after a comprehensive DC wafer-probing, then scribed for die-separation. These processes give good IC yield, with greater than 50% DC yield and greater than 80% RF yield (from visual) being observed. The IC was fabricated using normal and higher doped vapor phase epitaxial materials (Nch = $3.0E17cm^{-3}$, and $4.2E17cm^{-3}$ respectively) to compare the difference in performance. A photograph of a completed MMIC chip is shown in Fig 2. The chip measures 1.5mm x 1.8mm.

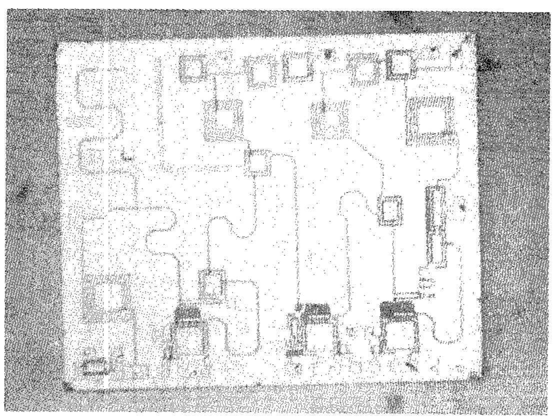


FIGURE 2 PHOTOGRAPH OF THE MMIC CHIP

MEASURED PERFORMANCE

Figure 3 shows the results of a chip fabricated using normal doped material. The amplifier exhibits 11.5 +/- 1.5dB gain across the 5-20 GHz bandwidth at a single DC bias of +3.0V, 60mA. The input VSWR is less than 2.0:1 and the output VSWR is less than 2.5:1 over the entire bandwidth. The reverse isolation is greater than 30dB. Figure 4 shows the performance of the chip using higher doped material. The VSWR is similar to that of the normal doped chip while the gain is 2dB higher, and the total DC bias current is only 40mA. The current to gain efficiency (3.3mA/dB) of the high gain chip is the highest ever reported for a monolithic amplifier operating over this bandwidth.

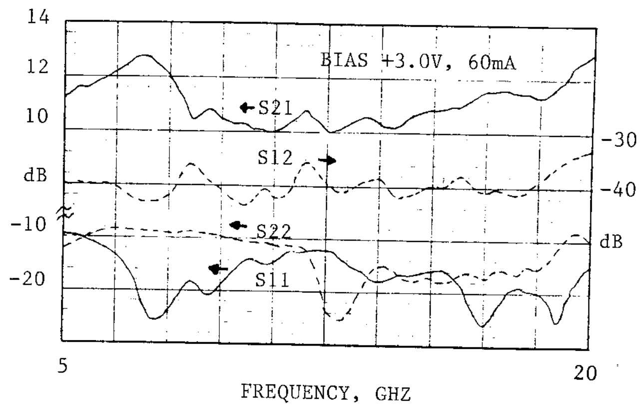


FIGURE 3 MEASURED PERFORMANCE OF A NORMAL DOPED IC CHIP

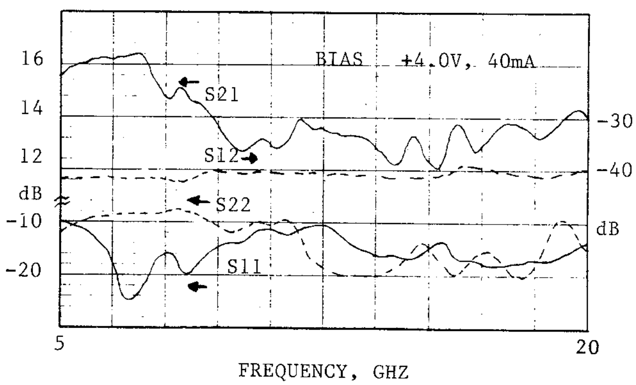
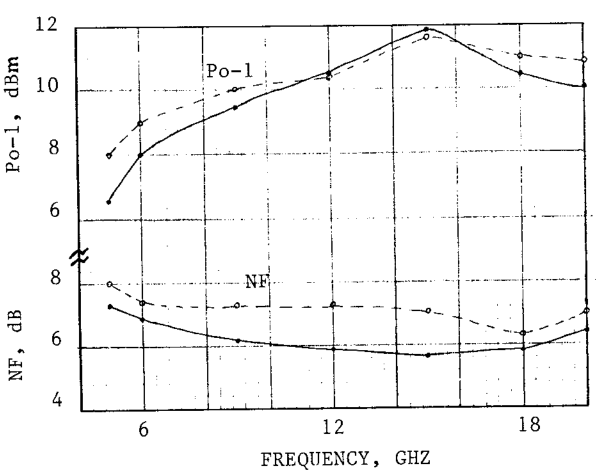


FIGURE 4 MEASURED PERFORMANCE OF A HIGH DOPED IC CHIP (N_{ch} = 4.2 x 10^{17} x cm^{-3})

The power output and noise figure performances of the MMIC chips are shown in Figure 5. Both chips exhibit greater than 10dBm 1dB-compressed power output at and beyond the middle frequency. The power outputs at the low frequency end are about 2dB lower, attributed primarily to the IC output matching characteristics. The high doped chip measures less than 6.5dB noise figure over most frequencies in the bandwidth. The normal doped chip has noise figure about 0.8dB higher. This is attributed to the difference in device transconductance and the DC bias current level. The MESFET transconductances of the high and normal doped chips are measured to be about 180mS/mm and 140mS/mm respectively.

The middle stage, in addition to increasing the amplifier gain and reverse isolation, also provides a gain control port with negligable effect on the amplifier's input and output stages. The AGC characteristics and the IC noise figure variation with AGC are shown in Figures 6 and 7 for the high doped chip (the AGC performances of the normal doped chip are similar). As indicated, the middle stage AGC provides greater than 10dB gain control without much effect on the amplifier's matching and, with a 3dB gain control, the amplifier's noise figure variation is less than 0.2dB. These features of the AGC will be useful for amplifier gain control and temperature compensation. The IC gain variation with temperature, measured from 5-18.6 GHz, was observed to be about +/- 2dB over -54 to +95°C temperature range.



-------: normal doped chip, DC bias at +3.0V, 60mA

———: high doped chip, DC bias at +4.0V, 40mA

FIGURE 5 POWER OUTPUT AND NOISE FIGURE PERFORMANCE OF THE MMIC

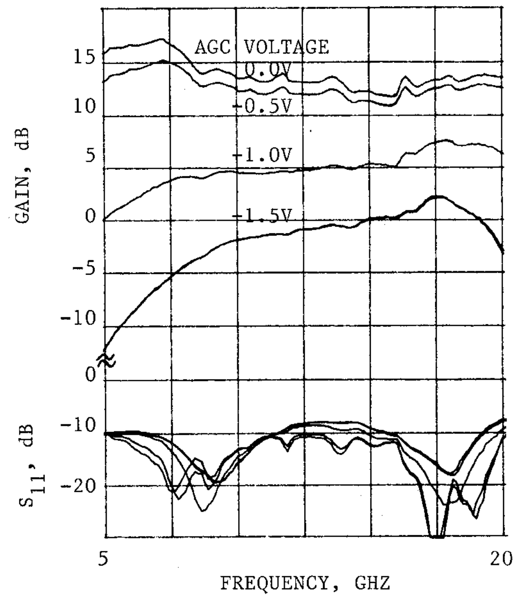


FIGURE 6 AGC CHARACTERISTICS OF THE HIGH DOPED MMIC

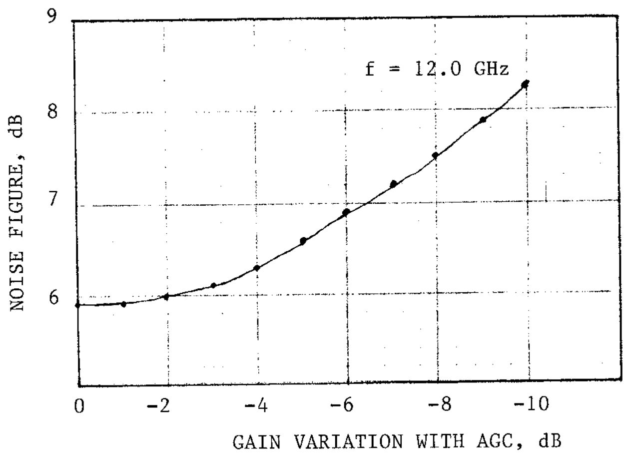


FIGURE 7 NOISE FIGURE AS A FUNCTION OF AGC FOR THE HIGH DOPED MMIC

CONCLUSION

A low current, high gain monolithic amplifier has been designed and measured. The IC, employing a three-stage (feedback-reactive-feedback) configuration, exhibits low current, high gain, fair VSWR, high reverse isolation, and a separate AGC over a broad 5-20 GHz bandwidth. The state-of-the-art gain efficiency of the IC is greater by at least a factor of 2 than those generally available with a distributed approach using more complex devices and processes. Compared to a two-stage feedback approach (5), the current to gain efficiency is favorable and the amplifier VSWRs and gain-bandwidth are better. The middle stage also provides a greater than 10dB gain control with minimal degradation of the IC noise figure and input/output matches.

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